

VLSI Design of Fixed-Width Booth Multiplier by using Multilevel Conditional Probability

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ABSTRACT- This brief proposes a precision modification fixed width Booth multiplier that remunerates the truncation mistake utilizing a multilevel conditional probability (MLCP) estimator and determines a shut frame for different piece widths L and section data w. Contrasted and the comprehensive recreations technique, the proposed MLCP estimator significantly decreases reenactment time and effectively changes exactness dependent on numerical inferences. In contrast to past restrictive likelihood techniques, the proposed MLCP utilizes whole nonzero code, to be specific MLCP, to appraise the truncation blunder and accomplish higher precision levels. Besides, the basic and little MLCP repaid circuit is proposed in this brief. The consequences of this concise demonstrate that the proposed MLCP Booth multipliers accomplish ease high exactness execution.

Record Terms—Fixed-width Booth multiplier, multilevel conditional probability (MLCP), truncation mistake

I. INTRODUCTION

Settled width multipliers are broadly utilized in computerized flag handling (DSP) applications [1]– [4], for example, quick Fourier change [2] and discrete cosine change [3], [4]. To produce a yield with indistinguishable width from the information, settled width multipliers truncate the half minimum huge bits (LSBs) in DSP applications. Consequently, truncation mistakes can happen in fixed width multiplier structures. The settled width multiplier with most noteworthy precision is known as a post truncated (P-T) multiplier, which truncates half of the LSBs results in the wake of computing all items. In any case, a P-T multiplier requires an expansive circuit territory to ascertain truncation part items. On the other hand, a direct-truncated (D-T) multiplier truncates half of the LSBs items straightforwardly to ration circuit region, however creates an expansive truncation mistake.

Table i
Mapped table of a modified booth encoder

b_{2i+1}	b_{2i}	b_{2i-1}	y_i	z_i	y_{i-1}
0	0	0	0	0	
0	0	1	1	1	-1, -2
0	1	0	1	1	1, 2
0	1	1	2	1	-1, -2
1	0	0	-2	1	1, 2
1	0	1	-1	1	-1, -2
1	1	0	-1	1	1, 2
1	1	1	0	0	

To accomplish a reasonable plan between exactness (P-T) and zone cost (D-T), a few analysts have displayed different blunder repaid circuits to mitigate the truncation mistakes in Baugh– Wooley (BW) multipliers [5]– [10] and Booth multipliers [11]– [21]. Since a couple of items are truncated after Booth encoding, the multipliers have a littler truncation blunder than that of BW multipliers [17]. In this manner, numerous past works have concentrated on the repaid circuit in Booth multipliers [11]– [21]. Tune et al. [18] present a twofold edge dependent on factual investigation. Their remunerated circuit devours an extensive circuit territory due to the mind boggling bend fitting required for measurable examination. Wang et al. utilize more item data to enhance exactness, yet their comprehensive recreation required a lot of built up time. To lessen the built up time for remunerated circuits, Li et al. [20] present likelihood estimator (PEB) that significantly lessens figuring time. A versatile restrictive likelihood estimator (ACPE) [21] is exhibited to enhance the precision utilizing contingent likelihood to additionally prompt the section data w for modifying the precision when connected to kinds of DSP frameworks. In this manner, two kinds of repaid circuits for different w are presented in [18], and the summed up type of PEB is exhibited in [17]. In whole, the built up time for remunerated circuits and alteration are basic to settled width Booth multipliers.

This brief proposes a precision change settled width Booth multiplier that utilizes the staggered restrictive likelihood (MLCP) technique to execute the repaid circuit. The MLCP strategy creates a shut frame with different bit widths L and segment data w; hence, the repaid circuit can be set up rapidly, and the precision can be balanced by evolving w. Rather than the contingent likelihood technique for ACPE [21], which utilizes single nonzero code to gauge truncation blunders, the proposed MLCP produces appraises by utilizing all nonzero code, which shows elevated amounts of inter correlation. In spite of the fact that MLCP strategy has higher intricacy to appraise truncation blunders when contrasted and ACPE one, the exactness of MLCP technique is higher than that of ACPE strategy. Besides, straightforward and little repaid circuits are proposed from a solitary remunerated shut frame. As indicated by the tradeoff among precision and circuit region, the MLCP technique gives a harmony

among exactness and circuit zone. The execution consequences of this concise demonstrate that the proposed MLCP Booth multiplier accomplishes ease highaccuracy execution. The rest of this brief is sorted out as pursues. Area II shows the basic inference for a Booth multiplier. The determination and design of the proposed MLCP estimator are tended to in Section III. Area IV presents examinations and a talk of these methodologies, and Section V gives the end.

II. Fixed-width modified booth multiplier

Adjusted Booth encoding is ordinarily utilized in multiplier structures to diminish the quantity of incomplete items. [22].The2L-bit product P can be expressed in two's complement.

Table ii
Partial products for an eight-bit booth encoder

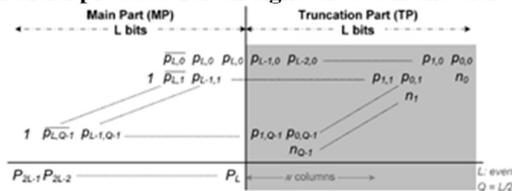


Fig.1. Partial product array for Booth multiplier. Representation as follows:

$$\begin{aligned}
 A &= -a_{L-1}2^{L-1} + \sum_{i=0}^{L-2} a_i \cdot 2^i \\
 B &= -b_{L-1}2^{L-1} + \sum_{i=0}^{L-2} b_i \cdot 2^i \\
 P &= A \times B.
 \end{aligned}
 \tag{1}$$

Table I records three connected sources of info b_{2i+1} , b_{2i} , and b_{2i-1} mapped into y_i utilizing a Booth encoder, in which the nonzero code z_i is a one-piece digit of which the esteem is resolved by whether y_i squares with zero and z comprises of z_i . Table II demonstrates the incomplete items with relating y_i for an eight-piece Booth encoder. Subsequent to encoding, the halfway item cluster with an even width L contains $Q = L/2$ lines.

Fig. 1 demonstrates the halfway item cluster in a Booth multiplier for actuating the section data w , where w shows the quantity of genuine item segments incorporated into the remunerated circuit.

III. PROPOSED MLCP ESTIMATOR

The quantized product P_q for a fixed-width multiplier can be expressed as follows

$$P \approx P_q = MP + TP = MP + \sigma \cdot 2^L \tag{2}$$

where MP is the principle part of multiplier, which utilizes genuine halfway items to compute results; TP is the truncation part (Fig. 1, shaded locale), which will be truncated utilizing fixed

width duplication; and σ speaks to the remunerated inclination of the MLCP estimator, which comprises of TP_{mj} and TP_{mi} parts by playing out the adjusting activity $Round()$.

$$\sigma = Round (TP_{mj} + TP_{mi}). \tag{3}$$

The real term TP_{mj} gives genuine data and the minor term TP_{mi} can be evaluated dependent on the proposed MLCP strategy. Along these lines, the remunerated inclination σ can be summed by acquiring TP_{mj} and evaluating TP_{mi} .

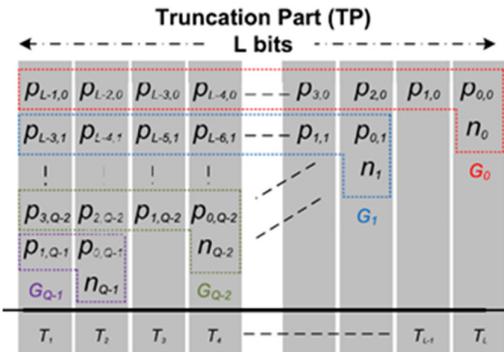


Fig. 2. Truncation part of the proposed Booth multiplier.

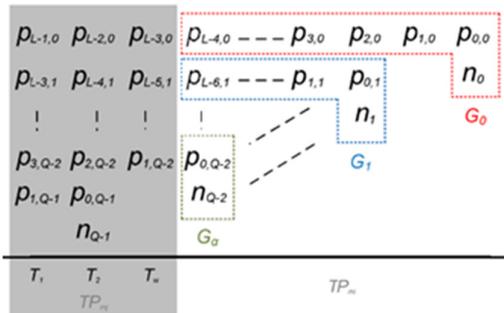


Fig. 3. G set of the proposed Booth multiplier with w = 3.

A. Derived MLCP Formula

Fig. 2 demonstrates that the TP can be parceled into encoding aggregate set (G) and section set (T). The encoding bunches in G are characterized as pursues:

$$\begin{aligned}
 G_0 &= 2^{-L}(p_{0,0} + n_0) + \dots + 2^{-1-w} p_{L-1-w,0} \\
 G_1 &= 2^{-(L-2)}(p_{0,1} + n_1) + \dots + 2^{-1-w} p_{L-3-w,1}
 \end{aligned}$$

⋮

$$G_{Q-1} = 2^{-2}(p_{0,Q-1} + n_{Q-1}) \tag{4}$$

and the column groups in T set are defined as follows.

$$\begin{aligned}
 T_1 &= 2^{-1}(p_{L-1,0} + p_{L-3,1} + \dots + p_{1,Q-1}) \\
 T_2 &= 2^{-2}(p_{L-2,0} + p_{L-4,1} + \dots + n_{Q-1}) \\
 &\vdots \\
 T_L &= 2^{-L}(p_{0,0} + n_0).
 \end{aligned}
 \tag{5}$$

With the column information w , the terms TP_{mj} and TP_{mi} can be expressed as the following equations

$$TP_{mj} = T_1 + T_2 + \dots + T_w \tag{6}$$

$$TP_{mi} = G_0 + G_1 + \dots + G_\alpha \tag{7}$$

where $\alpha = Q-1-w/2$, $_$ speaks to the ground surface activity,

TP_{mj} is built by summing T_i ($w \geq 1 \geq 1$), and TP_{mi} comprises of G_j , ($\alpha \geq j \geq 0$). Note that the G set changes dependent on the section data w . Fig. 3 demonstrates a case for TP , where $w = 3$.

The MLCP technique proposed in this brief includes utilizing the nonzero code z to set up a MLCP estimator. The normal qualities on all components in TP_{mi} with relating nonzero code are inferred first. Rather than the technique in [21], the proposed MLCP strategy includes utilizing nonzero code to evaluate TP_{mi} . Subsequently, more truncation blunders can be lessened contrasted and [21], which includes utilizing just a single nonzero bit. For instance, the qualities $L = 8$, $w = 1$, and $z = 1111$ can be utilized to figure the normal estimation of $p_{0,1} E[p_{0,1}|z = 1111]$.

$$\begin{aligned} &= P[p_{0,1} = 1]P[p_{0,1}|z_1 = 1]P[z_1 = 1|z_0 = 1] \\ &= \sum_{m=\pm 1, -2} \left(\sum_{n=\pm 1, \pm 2} P[p_{0,1} = 1] \right. \\ &\quad \left. \times P[p_{0,1}|y_1 = n]P[y_1 = n|y_0 = m] \right) \\ &= \left(1 \times 0 + \frac{1}{2} \times \frac{1}{3} + \frac{1}{2} \times \frac{1}{3} + 0 \times \frac{1}{3} \right)_{m=-2} \\ &\quad + \left(1 \times 0 + \frac{1}{2} \times \frac{1}{3} + \frac{1}{2} \times \frac{1}{3} + 0 \times \frac{1}{3} \right)_{m=-1} \\ &\quad + \left(1 \times \frac{1}{3} + \frac{1}{2} \times \frac{1}{3} + \frac{1}{2} \times \frac{1}{3} + 0 \times 0 \right)_{m=1} \\ &= \frac{4}{9}. \end{aligned} \tag{8}$$

B. Proposed Generalized MLCP Format

With the derivation of the MLCP method, the expected value of each part in TP_{mi} can be estimated as follows:

$$\begin{aligned} TP_{mi} &= TP_0 + \dots + TP_\alpha \\ &\simeq E[(TP_0 + \dots + TP_\alpha)|z] \\ &= E[TP_0|z] + E[TP_1|z] + \dots + E[TP_\alpha|z] \\ &= E[TP_0|z_0] + E[TP_1|z_1, z_0] + \dots + E[TP_\alpha] \\ &= E_0 + E_1 + \dots + E_\alpha \end{aligned}$$

where the contingent expected qualities $E_0, E_1, \dots, E_\alpha$ depend significantly on the nonzero code nz . In this way, the restrictive expected esteem can be evaluated utilizing (9), and which yields three cases for the normal estimation of TP_{mi} .

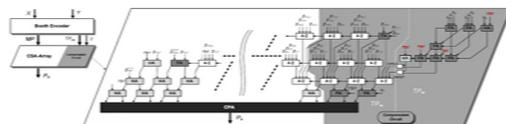


Fig. 4. Architecture of the proposed MLCP Booth multiplier for L = 16 and w = 3.

Since just the convey spread from TP_{mi} to TP_{mj} must be considered, the normal estimation of TP_{mi} can be improved as

$$TP_{mi} = \sum_{i=0}^{\alpha} E_i \simeq \text{Sone} \times 2^{-w}$$

C. Architecture of the Proposed MLCP Booth Multiplier

With the proposed MLCP equation in (20), the repaid predisposition σ can be acquired with the relating L what's more, w . Fig. 5 demonstrates that the proposed MLCP Booth multiplier has a Booth encoder tended to and a convey spare snake (CSA) cluster with 4- 2 and 3- 2 blowers. The repaid circuit entireties TP_{mj} and TP_{mi} all together. The proposed MLCP repaid circuit executes utilizing CSA engineering and the capacity of subtracting one is planned by including every one of the one values for twos supplement portrayal. Utilizing $L = 16$ and $w = 3$ for instance, the Sone in (19) can be expressed as pursues:

$$\text{Sone} = \left\lfloor \frac{\beta + 4'b1111}{2} \right\rfloor$$

The proposed MLCP circuits rely upon α , in this manner, different word lengths L and section data w can utilize the equivalent MLCP circuit. Utilizing $\alpha = 6$ for instance, the MLCP circuit (Fig. 5) can be utilized, yielding $L = 16$ with $w = 3$, $L = 16$ with $w = 2$, and $L = 14$ with $w = 1$, etc. Fig. 5 demonstrates the utilization of the MLCP circuit with relating w

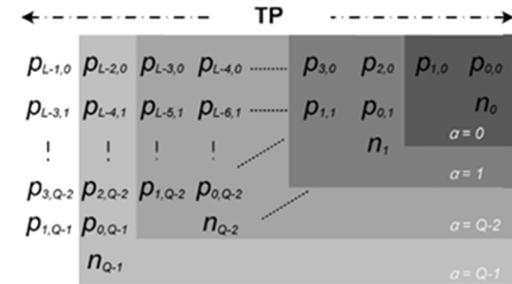


Fig.5.Usage of MLCP circuit with corresponding.

Since the proposed MLCP technique involves utilizing the contingent likelihood strategy, it yields extensive time put something aside for the repaid circuit contrasted and the thorough and tedious heuristic reproduction strategies. In this manner, the proposed MLCP remunerated circuit can undoubtedly execute a substantial bit width (as $L > 16$) Booth multiplier and modify precision by changing the segment data w .

CHAPTER-IV RESULTS AND DISCUSSIONS

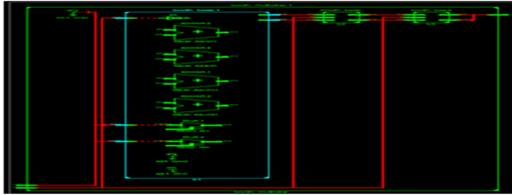


Fig6: RTL Schematic for the proposed design

V. CONCLUSION

This short introduces a shut MLCP equation that incorporates section data w to change exactness relying upon framework prerequisites. This equation is inferred without performing tedious and comprehensive recreations, and can be connected to extensive Booth multipliers to accomplish high-precision execution. Hence, the proposed MLCP repaid circuit can be utilized to build up a high-precision, ease, and adaptable settled width Booth multiplier.

REFERENCES

- [1] K. K. Parhi, VLSI Digital Signal Processing Systems: Design and Implementation. New York, NY, USA: Wiley, 1999.
- [2] S. N. Tang, J. W. Tsai, and T. Y. Chang, "A 2.4-Gs/s FFT processor for OFDM-based WPAN applications," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 57, no. 6, pp. 451–455, Jun. 2010.
- [3] S. C. Hsia and S. H. Wang, "Shift-register-based data transposition for cost-effective discrete cosine transform," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 15, no. 6, pp. 725–728, Jun. 2007.
- [4] Y. H. Chen, T. Y. Chang, and C. Y. Li, "High throughput DA-based DCT with high accuracy error-compensated adder tree," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 19, no. 4, pp. 709–714, Apr. 2011.
- [5] L. D. Van and C. C. Yang, "Generalized low-error area-efficient fixed width multipliers," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 52, no. 8, pp. 1608–1619, Aug. 2005.
- [6] L. D. Van, S. S. Wang, and W. S. Feng, "Design of the lower error fixed-width multiplier and its application," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 47, no. 10, pp. 1112–1118, Oct. 2000.
- [7] C. H. Chang and R. K. Satzoda, "A low error and high performance multiplexer-based truncated multiplier," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 18, no. 12, pp. 1767–1771, Dec. 2010.
- [8] N. Petra, D. D. Caro, V. Garofalo, E. Napoli, and A. G. M. Strollo, "Truncated binary multipliers with variable correction and minimum mean square error," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 57, no. 6, pp. 1312–1325, Jun. 2010.
- [9] N. Petra, D. D. Caro, V. Garofalo, E. Napoli, and A. G. M. Strollo, "Design of fixed-width multipliers with linear compensation function," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 58, no. 5, pp. 947–960, May 2011.

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