Implementation of high performance SRAM Cell Through Transmission Gate

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Abstract- *Static Random Access Memory (SRAM) plays a most substantial role in the microprocessor world, but as the technology is scaling down in nanometers, leakage parameters and delay are the most common problems for SRAM cell which is basically designed for very low power application. Transmission gate is used to further reduced leakage current penetrating in the 8T SRAM cell. Comparative analysis is performed by using transmission gate. This paper represents a method for design a variability aware SRAM cell. The proposed architecture of the TG8T SRAM cell is analogous to the standard 6T SRAM cell, theonly exception is that they possess full transmission gates which replace an access pass transistor. The paper studies the different parameters of TG8Twrite operation at 0.7 V like leakage current is 229.2fA, leakage power is 297.4nW, delay is 20.92ns and SNR is 4.77dB. This result performs on the cadence virtuoso tool at 45nm technology.*

Keywords- **SRAM, TG8T, leakage current, leakage power, delay.**

I. INTRODUCTION

The continuous scaling down of bulk CMOS create major issues due to it base material. The primary obstacles to the scaling of bulk CMOS to 32nmgatelengths include short channel effects, Sub-threshold leakage, gate-dielectric leakage and device to device variations. Due to sudden increase in threshold voltage i.e. V oscillation produced by overall and general process variations occur in ultra-short- channel devices, 6T SRAM cell and their modifications cannot be operated at advance scaling of supply voltages without functional and parametric failure causes yield loss. The design of standard 6T SRAM cell undergoes a lot of problem on write delay [1].The design of Low power 6T SRAM cell could decrease the write power and access delay [2] but could not improve their stability. In deep submicron ranges, none of the earlier works has studied about the improvement of variability in SRAM cell at the schematic level. Therefore, we design a vigorous and variation accepting SRAM cell design technique capable of gripping Vt shift due to random doping fluctuation(RDF), and variation in further device and their process parameters (such as length, width, sub-wavelength-lithography, oxide thickness, etching, and annealing) and still be able to perform expected functions need to be investigated. To fulfill this drawback we propose a transmission gate 8T SRAM cell (TG8T) and compare their performance with standard 6T SRAM cell at cadence virtuoso tool at 45nm technology.

The rest of the paper is designed as follows. Section 2 shows the proposed design and its operation. Section 3 shows the simulation result and their comparison with standard 6T SRAM cell. At last we show the conclusion in Section 4.

II. PROPOSED TRANSMISSION GATE BASED 8T SRAM CELL (TG8T)

This fragment shows the proposed architecture of TG8T SRAM which is resembles to the standard 6T SRAM cell.

A. Architecture of TG8T SRAM cell

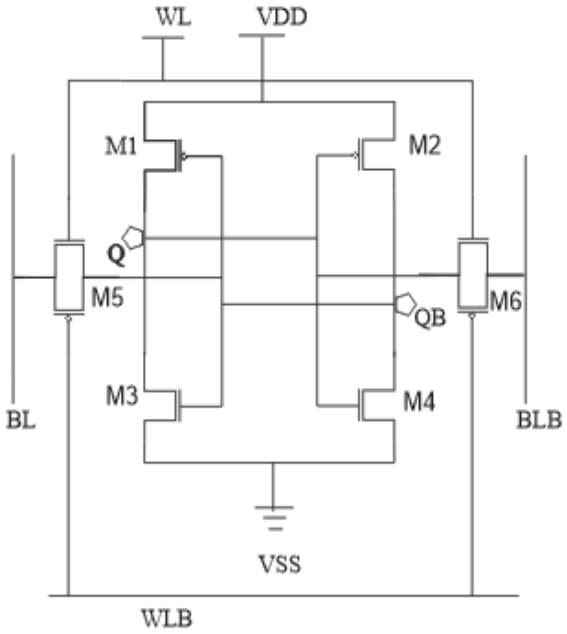

Fig.1 Proposed TG-based fully 8T SRAM cell (TG8T).

The main motive behind the forceful device scaling is to achieve enriched performance and increase ranges, none of the earlier works has studied about the integration. These improvements led to the cost of increased sensitivity to standby leakage, delay mostly in area-constrained circuit such as SRAM that requires minimum-geometry devices[3]. In this work, an effort has to be done to solve these problems in conventional 6T SRAM cell by considering minimum area consequences and achieve its fully differential architecture. This paper proposes a design of TG-based fully differential 8T SRAM cell (Fig.1) and their design metrics shows in the conventional 6T SRAM cell shown at Fig.2.

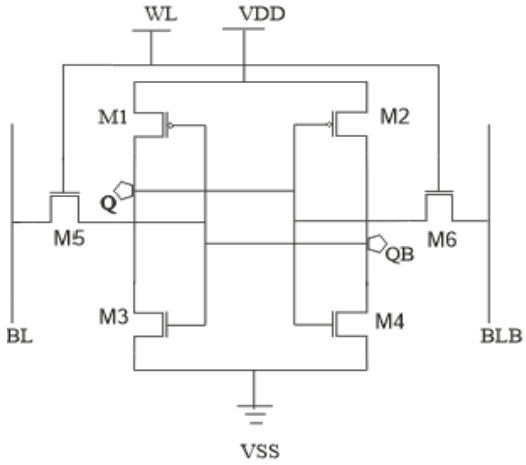

Fig.2 Architecture of Standard 6T SRAM cell.

TG8T uses differential operation and does not possess as much architectural changes except adding a PMOS in parallel with each access NMOS in conventional 6T SRAM cell shown by M5 and M6, by this we make it TG8T SRAM cell. An additional control WLB is required for switching the access PMOS. The WLB and WL (word line) are non-overlapping opposite signals. Therefore, during read and write operation, to retrieve the data from cell all access FETs are swapped simultaneously. But, during hold mode all access FETs remain shot off.

B. Working of TG8T SRAM cell.

The working of TG8T SRAM cell consist of two operation i.e. write and read operation.

When we performing a write operation ,both the bit lines are at opposite voltages which represent if bit line BL is at high then BLB is at low and vice versa (BL=1 and BLB =0 or BL =0 and BLB =1). When WL becomes high and also WLB =0 which enables NMOS and PMOS transistors M5 and M6 then data writes on the output nodes Q and QB of back to back connected inverter.

When we perform the read operation which is just opposite to the write operation, both the bit lines are at high voltages also behave as an output and WL is raised to high and WLB at 0. Since one of the output nodes (Q and QB) is at low then one of pre-charged bit lines start discharging and at that instant data is going to be read.

III. SIMULATION RESULTS

The main focus of this work is to meet all challenges faces in designing of memory circuit at nanoscale technology, where deviations arisesdue to process and environmental parameters such as operating voltage and temperature. The basic cause of variations is scaling. The leakage current of TG8T SRAM cell is improved as compared to conventional 6T SRAM cell. This paper attempts to minimize leakage parameters by using transmission gates and also improve their signal to noise ratio.

TABLE I Comparison of parameters of TG8T SRAM cell with 6T SRAM cell.

Parameters	Conventional 6T SRAM	Transmission gate 8T SRAM (TG8T)
	Write	*Write*
Leakage current	69.22×10^{-12} A	229.2×10^{-15}A
Leakage power	7.346nW	2.97nW
Delay	20.57 ns	20.92 ns
SNR	1.58dB	4.77dB

A. Leakage Current

As the scaling of gate length is done, the device leakage increases exponentially with technology generations. For SRAM cell, the leakage current is the main basis of standby power consumption whose major components are the sub- threshold leakage, the reverse biased band-to-band tunneling junction leakage andthe gate direct tunneling leakage in nano-scale devices [4].

1. Sub-threshold leakage

When the voltage across gate-source terminal is less than the threshold voltage (Vgs < Vth) the current flowing is referred as Sub-threshold leakage [5].
In the off state, a significant leakage current component is present in the weak inversion of CMOS transistor.

Isub = tech exp ((1)

This is direct exponentially relation with the threshold voltage, which provides the large sub threshold current in Short channel devices [6].

For calculating the leakage current, we have to connect one extra NMOS transistor to the ground of the circuit in architecture of 6T and 8T SRAM cell. In both 6T and 8T SRAM CELL, the bit lines are at VDD and WL which is low during standby mode. In this mode the NMOS transistor will have gate leakage. When sub-threshold current is in OFF state then transistor M2 and M3 will show sub-threshold leakage. This behavior signifies that it residues for a variety of programs under different Conditions about memory cell sizes, organization and instruction set architectures [7-8].

2. Junction tunneling leakage

It has two components one results from diffusion of carriers near the edges of the depletion region and other results from electron-hole pair generation which takes place in depletion region during reverse biasing. The junction tunneling current is defined as an exponential function of the reverse bias voltage across the junction and its doping.

3. Gate tunneling leakage

Tunneling of electrons from bulk silicon is present in NMOS/ PMOs transistor through the gate oxide layer into agate terminal gives rise to the gate tunneling effect. It composed of three constituents i.e. gate to drain overlap current, gate to source and gate to channel current (part of which goes to source and rest of the part goes to drain), gate substrate current. In CMOS technology, the leakage current from gate to substrate is very much lower in magnitude as compared to the overall gate to channel tunneling current always dominates the gate leakage in the OFF condition of the transistor. However, the gate to channel tunneling effect causes the gate current during ON condition. Since the gate to source and gate to drain overlap regions are much smaller than the gate tunneling current from OFF condition to ON condition.

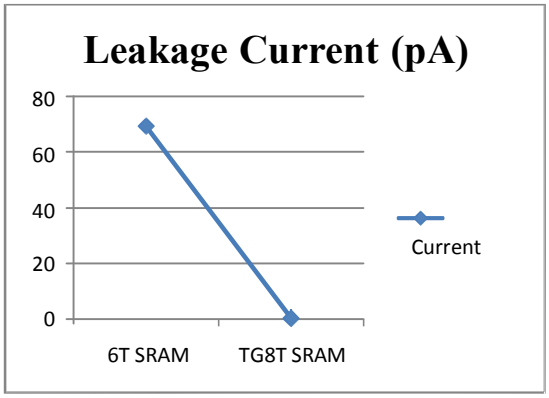

Fig.3 shows the Comparison of leakage current in 6T SRAM cell and TG8T SRAM cell at 0.7V.

B. Leakage power

Whenever the CMOS inverter is in stable mode, it has its PMOS and NMOS transistor shot off. There is no flow of current from power supply towards the ground. However, there is small current flowing through the Shot off transistor giving rise to leakage power consumption, shown by equation 1.

$$P = I_{leak} \times V_{dd} \qquad (2)$$

The static and dynamic power together results to the overall power consumption which is shown by the equation 3

$$P = ACV^{2}f + I \quad V \qquad (3)$$

During charging and discharging action of the capacitive load, the first term reflects the dynamic power loss, A reflects the fraction of gates which are actively switching whereas C is the total capacitive load for all gates. The second term is contributed by the static power loss which results from leakage current.

Where P is leakage power, Ileak is leakage current and Vdd is supply voltage. This equation obviously shows that leakage power is depends on supply voltage. Therefore, by lowering the supply voltage we can also control the power consumption in the circuit.

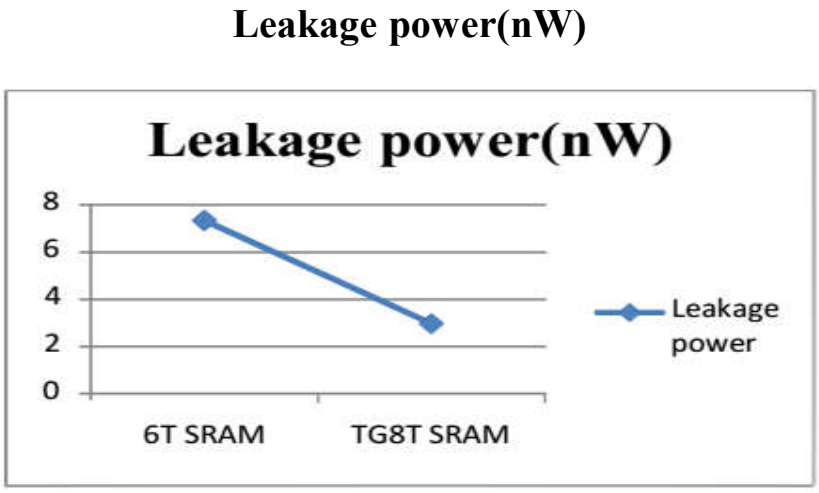

Fig.4 Comparison of leakage power of 6T SRAM cell and TG8T SRAM cell at o.7V

C. Delay

To determine delay of signal from input to output circuit during the high to low and vice versa at the output we use propagation delay times PHL and PLH [9].

We can define the PHL is referred to the time delay which occurs with the 50% of the voltage transition of the rising input voltage and falling output voltage. Similarly, we can define the PLH is referred to the time delay which occurs voltage and rising output voltage. Due to this assumption PHL becomes the time consumed for the output voltage to the time consumed for output voltage to rise from V_{OL} to 50% of the voltage level. The 50% of the voltage point is
defined by

$$V_{50\%} = V_{OL} + -(V_{OH}-V_{OL}) = -(V_{OH}+V_{OL}) \qquad (4)$$

Now we can define the average propagation delay P of the inverter which gives the average time required for the input signal to propagate through the inverter[10]-[11].

$$_{P} = \qquad (5)$$

Delay of the cell depends upon the time elapsed between the cell from input to output transition of the signal [12].

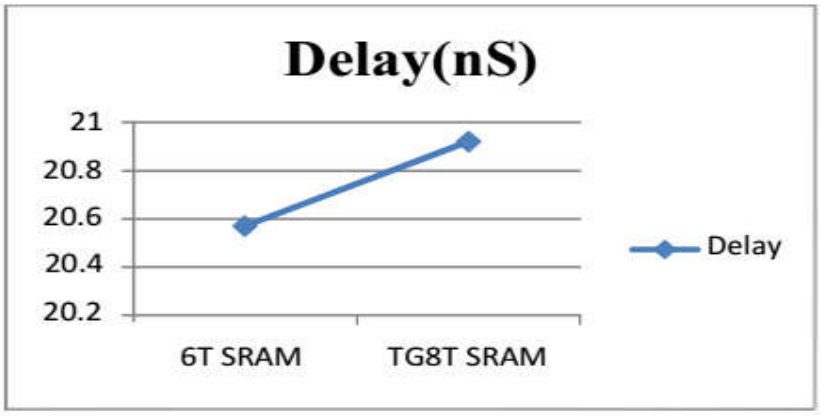

Fig.5 Comparison of delay in 6T SRAM cell and TG8T SRAM cell at 0.7V.

D.Signal to Noise ratio

Signal-to-noise ratio (commonly known as SNR or S/N) is a measure used in science and engineering that compares the level of a desired signal to the level of background noise. It is defined as the ratio of signal power to the noise power, often expressed in decibels. A ratio higher than 1:1 (greater than 0 dB) indicates more signal than noise. While SNR is commonly quoted for electrical signals, it can be applied to any form of signal. Signal-to-noise ratio is defined as the power ratio between a signal and the background noise.

$$SNR = \frac{P_{signal}}{P_{noise}} \qquad (6)$$

where P is average power. Both signal and noise power system must be measured at the same and equivalent points in a, and within the same system bandwidth.

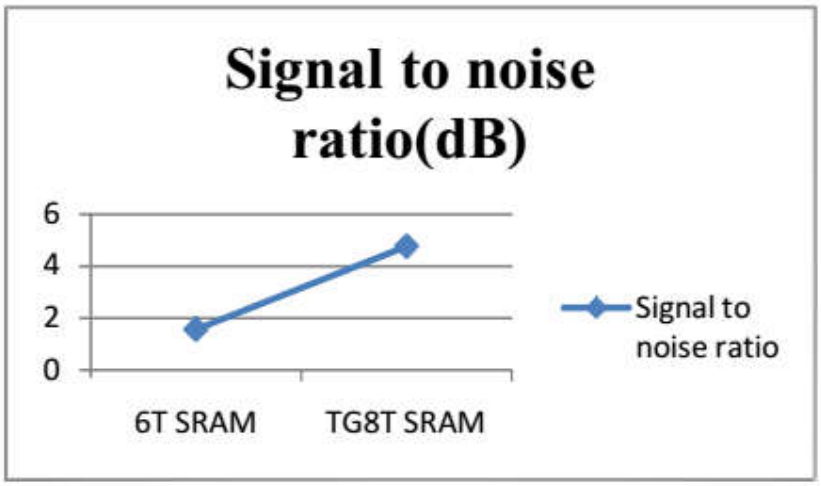

Fig.6 Comparison of SNR in 6T SRAM and TG8T SRAM cell.

IV. CONCLUSION

The scaling of CMOS technology has improved parameters by the benefit of high speed operation, reduced leakage parameters and also improved SNR in TG8T SRAM cell. In this paper I proposed a TG based 8T SRAM cell and also show their comparison with standard 6T SRAM cell. By comparing I conclude that in TG based 8T SRAM cell leakage current is reduced to 229.2fA, leakage power is reduced to 2.97 and SNR is improved to 4.77dB. Theresults show major enhancement in most of the design parameters over standard 6T SRAM cell signifying its strength and functionality.

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