DESIGN AND IMPLEMENTATION BRENT KUNG ARCHITECTURE USING VEDIC MULTIPLIER

S.Durgadevi, Dr.S.Anbukaruppusamy, Dr.N.Nandhagopal

Department of Electronics and Communication Engineering
Excel Engineering College, Komarapalayam,
Namakkal-637303, Tamilnadu, India.

Abstract— As multiplication influences the overall performance of system design, so the demand of high speed multipliers is increasing day by day. In this paper, Vedic multiplier using Brent Kung adder is designed. Architectures are proposed using parallel prefix adders. Instead of using dual Ripple Carry Adders (RCA), parallel prefix adder Brent Kung (BK) adder is used to design Regular Linear CSA. Adders are the basic building blocks in digital integrated circuit based designs. They work by creating two signals for each bit position, based on whether a carry is propagated through from a less significant bit position, generated in that bit position, or killed in that bit position. A proposed multiplier reduces delay .It is the advantage of proposed multiplier since it increases the speed. Delay of RCA is large therefore we have replaced it with parallel prefix adder which gives fast results. In this system, structures of 16-Bit Regular Linear Brent Kung CSA, Modified Linear BK CSA, Regular Square Root (SQRT) BK CSA and Modified SQRT BK CSA are designed. Power and delay of all these adder architectures are calculated at different input voltages.

Keywords- *RCA BK CLA (SORT).*

I. INTRODUCTION

Very large scale integration (VLSI) is the process of creating an integrated circuit (IC), combining thousands of transistors into a single chip. The strict limitation on power dissipation in any device must be met by the VLSI chip designer without compromising in their computational requirements[1]. The term Prefix means, the outcome of the operation depends on the initial inputs. Parallel adders involve the execution of an operation in parallel. This is done by segmentation into smaller pieces that are computed in parallel[2]. It is fast because the processing is accomplished in a parallel fashion. The Operation can be any arbitrary primitive operator that is associative is parallelizable.

Multipliers have been designed. But Vedic multiplier is the fastest multiplier (Vucha, 2014) .Among 16 sutras of Vedic mathematics; Urdhva Tiryagbhyam is a general formula which is applicable to all cases of multiplication. The speed of multiplier depends on type of adder. For high speed multiplication, fast adders are required. Parallel-prefix adders are known to have the best performance in VLSI designs. However, each type of parallel prefix adder has its own pros and cons and is chosen according to the design requirement of the application.

II. ADDERS

The most basic arithmetic operation that digital computers can performs addition of binary digits. In electronics, an adder or summer is a digital circuit that performs addition of numbers and is a fundamental building block in VLSI[3].

Adders are used not only in the arithmetic logic units but also in digital signal processor or any other kind of processors are used to calculate addresses and table indices Although adders can be constructed for many numerical representation such as binary coded decimal or excess code, the most common adders operate on binary numbers also in cases where two's complement or other complement is being used to represent negative numbers.

1.2TYPES OF ADDERS:

Adders can be broadly classified into two major categories namely,

- Serial Adders
- Parallel Adders.

1.3 SERIAL ADDER:

A serial adder is used to add binary number in serial form the two binary numbers to be added serially are stored in two shift registrar, b. Bits are added one pair at a time through a single full adder, Serial adder is done by a flip flop and a full adder .The carry out of the full adder is transferred to a D flip flop. The output of this flip flop is then used as the carry input for the next pair of significant bit. The sum bits from the S output of the full adder could transfer to a third shift register. By shifting the sum into a while the bits of A are shifted out, it is possible to use one register for storing both augends and sum of the bits .The serial input register b can be used to transfer a new binary number the addend bits are shifted out during the addition.

1.4 PARALLEL ADDER:

A binary parallel adder is digital circuits that adds two binary numbers in parallel form and produces the arithmetic sum of those numbers in parallel form .the full adder connected in a chain output carry from each full adder connected to the input carry of the next full adder in chain. The parallel adder classified into ripple carry adder, carry look-ahead adder[4].

2. BRENT KUNG ARCHITECTURE

The Brent–Kung adder is a parallel prefix form of carry look-ahead adder. It takes less area to implement than the Kogge adder. Regular layout with an aim of minimizing the chip area and ease of manufacturing. The Brent-Kung adder is the extreme boundary case of Maximum logic depth in PP adders (implies longer calculation time). Minimum number of nodes.

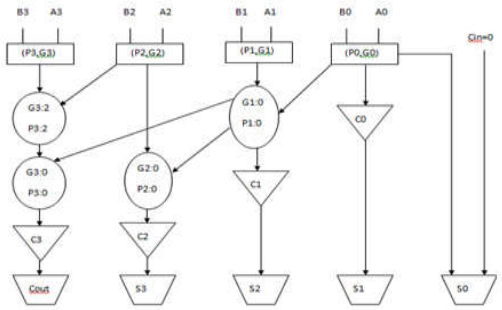


Figure 2 (a) Block Diagram Of Brent Kung Adder

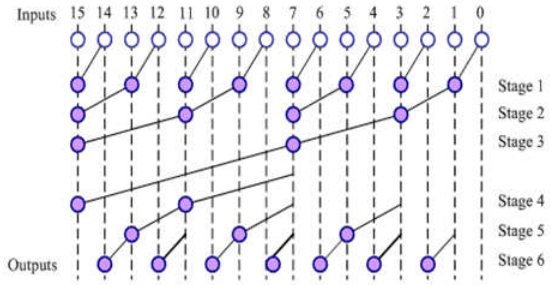


Figure 2 (b) Brent Kung adder (output)

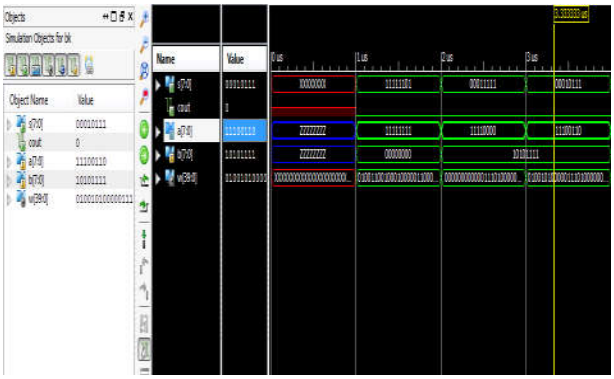


Figure 2 (c) Brent Kung adder (output)

In this there will be 8 inputs (a [0:7], [0:7] b) and equal number of outputs. We use 37 wires in this. To produce the output we will use generate and propagate operations[8].

2.1 16-BIT LINEAR MODIFIED BK CSA

Regular Linear Brent Kung Carry Select Adder uses single Ripple Carry Adder (RCA) for Cin=O and Brent Kung adder[8] for Cin=l and is therefore area-consuming. So, different add-one schemes like Binary to Excess- 1 Converter (BEC) have been introduced. Using BEC, Regular Linear BK CSA is modified in order to obtain a reduced area and power consumption. Binary to Excess-l converter is used to add 1 to the input numbers[9]. So, here Brent Kung adder with Cin=1 will be replaced by BEC because it require less number of logic gate for its

Implementation so the area of circuit is less. Linear Modified BK CSA is designed using Brent Kung adder for Cin=O and Binary to Excess-l Converter for Cin=l in order to reduce the area and power consumption with small speed penalty. Linear Modified BK CSA consists of 4 groups.

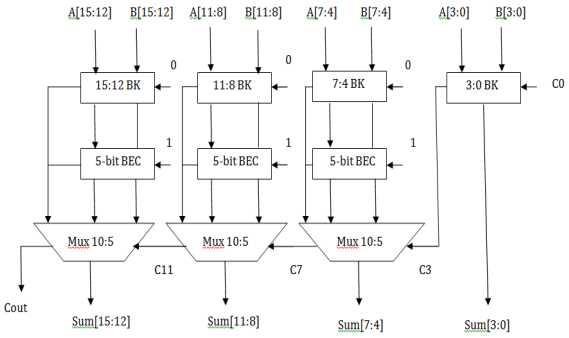


Fig 2.1(a) Block Diagram Of 16-Bit Linear Modified BK CSA

To replace the N-bit Brent Kung adder, aN+l bit BEC is required. The importance of BEC logic comes from the large silicon area reduction when designing Linear Modified BK CSA for large number of bits.

2.2 REGULAR SQUARE ROOT BRENT KUNG CARRY SELECT ADDER

Regular Linear Brent Kung Carry Select Adder consumes large area and to reduce its area a new design of adder is used i.e. Regular Square Root Brent Kung Carry Select Adder. Regular Square Root BK CSA has 5 groups of different size RCA for Cin=1 and MUX. High area usage and high time delay are the two main disadvantages of Linear Carry Select Adder. These disadvantages of linear carry select adder can be rectified by SQRT CSA. It is an improved version of linear CSA. The time delay of the linear adder can decrease, by having one more input into each set of adders than in the previous set. This is called a Square Root Carry Select Adder[2].

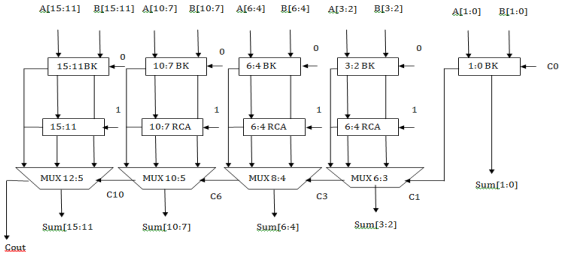


Figure 2.2 (a) Regular Square Root Brent Kung Carry Select Adder

2.3 MODIFIED SQUARE ROOT BRENT KUNG CARRY SELECT ADDER

Modified Square Root Brent Kung Carry Select Adder has been designed using Brent Kung adder for Cin=O and BEC for Cin=l and then there is a multiplexer stage. It has 5 groups of different size Brent Kung adder and Binary to Excess-l Converter (BEC). BEC is used to add 1 to the input numbers. Less number of logic gates are used to design BEC as compared to RCA therefore it consumes less area.

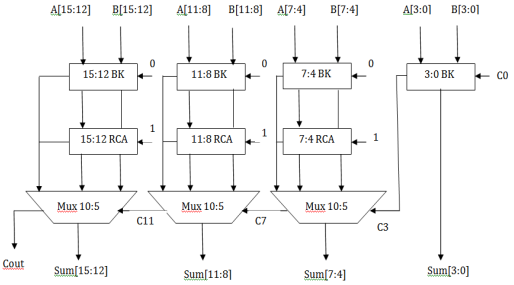


Figure 2.3(a) Regular Linear Brent Kung Carry Select Adder

2.4 Binary excess converter:

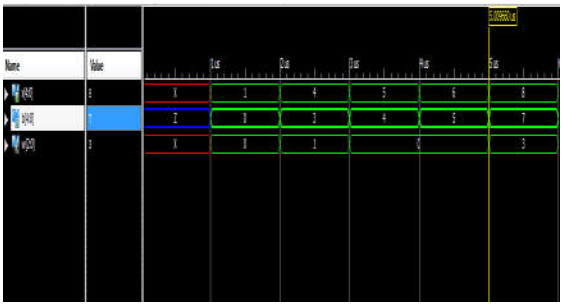


Figure 2.4(a) 10:5 Mux (Output)

By giving 4 inputs (B0 B1 B2 B3) the outputs obtained are (X0 X1 X2 X3) here we use 2 wire lines and for an inputs of 7 we get an output 8 that is the output exceeds input by the value of 1.

2.5 10:5 Mux:

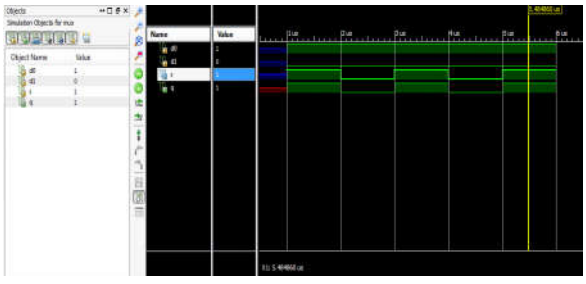
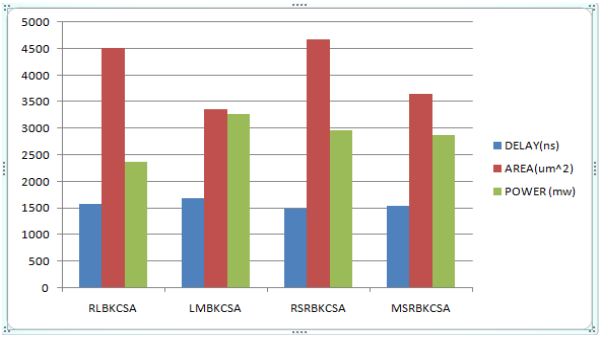


Figure 2.5(a) 10:5 Mux (Output)

In multiplexer we will give 2 inputs (do, d1) and there will be an single output (q).we will use single selection line whose when it is 0 1st output will be displayed when it is 1 the another one will be displayed

ADDERS	AREA (ns)	POWER (mw)	DELAY (um^2)
Regular linear BK CSA	4516	182375.81	1588
Linear Modified BK CSA	3364	193367.07	1688
Regular Square Root BK CSA	4676	81296.89	1485
Modified Square Root BK CSA	3655	89885.90	1550

2.6 Comparisons of parallel prefix adder:



2.7Bar Chart Comparisons of parallel prefix adder

3. VEDIC MULIPLIER

Discovered by Vedic's It mainly deals with Vedic mathematical formulae and their application to various branches of mathematics. Vedic mathematics in fast calculations. Multiplication, division, squaring, cubing, square, root, cube root, log, trignometry and exponential etc. The Vedic multiplier is numeric computations in easy and fast manner.

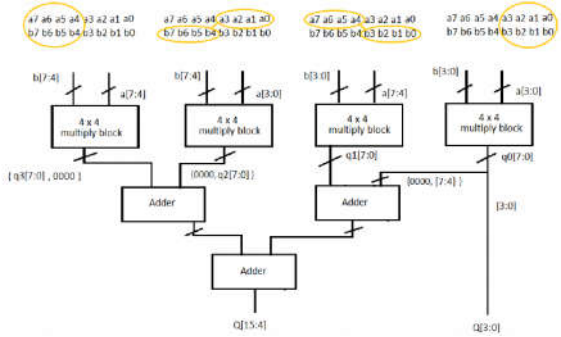
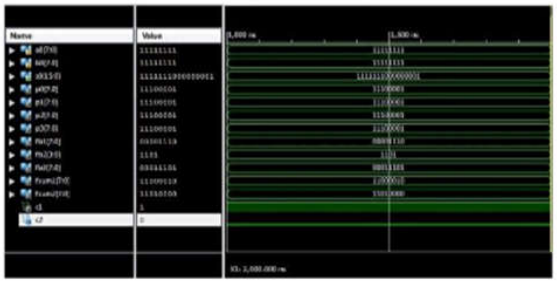


Figure 2 (a) Block Diagram Of Vedic Multiplier

Many such difficulties in learning Mathematics enter into a long list if prepared by an experienced teacher of Mathematics. Volumes have been written on the diagnosis of 'learning difficulties' related to Mathematics and remedial techniques. Learning Mathematics is an unpleasant experience to some students mainly because it involves mental exercise.

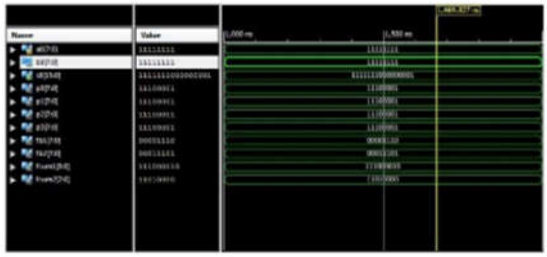
3.1 8BIT VEDIC MULTIPLIER USING ADDER

8-bit proposed Multipliers by combining Vedic Multiplier and parallel prefix adder. Used for systhesize the verilog codes of multipliers Since deviation is obtained by Nikhilam sutra a call the method as Nikhilam multiplication.



3.2 8BIT VEDIC MULTIPLIER USING BRENT KUNG ADDER

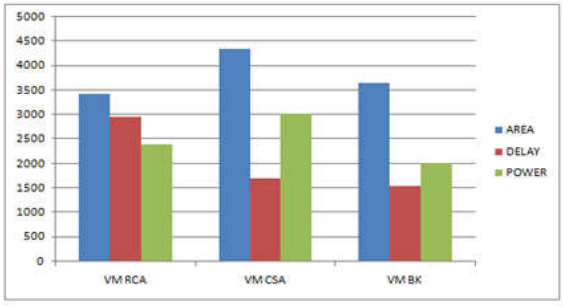
This is done by adding partial products using Brent Kung Adders based Vedic multiplier is found to have reduced delay and speed of BKA based multiplier is increased but the only limitation is that area is slightly increased.



The simulation result for 8bit Vedic Multiplier using MUX based adder is shown in figure in which a=11111111 and b=11111111 is taken and result is y=1111111000000001 is obtained.

PARAMETER	AREA (um^2)	POWER (mw)	DELAY (ns)
VM RCA	2421	2961.8	2391
VM CSA	4351	1703.5	3038
VM BK	3655	1550	2021

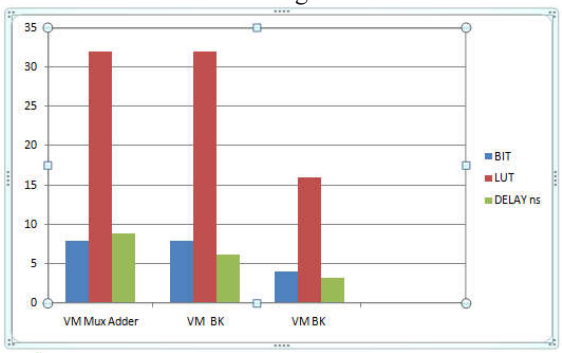
3.3 Comparisons of Vedic Multiplier and Brent Kung Adder



3.4 Bar Chart Comparisons of Vedic Multiplier and Brent Kung Adder

TYPE	BITS	LUT(um^2)	DELAY(ns)
Vedic Multiplier Using Mux Adder	8	32	8.894
Vedic Multiplier Using BK Adder	8	32	6.176
Vedic Multiplier Using Brent Kung Adder	4	16	3.165
	8	32	6.176

3.5 Comparisons of Bitwise Vedic Multiplier and Brent Kung Adder



3.6 Bar Chart Comparisons of Vedic Multiplier and Brent Kung Adder

CONCLUSION

This paper, novel high speed architecture for multiplication by combining the features of Vedic multiplier & Brent Kung adder is proposed. a Modified Square Root BK Carry Select Adder is proposed which is designed using single Brent kung adder and Binary to Excess-l Converter instead of using single Brent kung adder for C in=O and Ripple Carry Adder for C in=l in order to reduce the delay and power consumption of the circuit.

Here, the adder architectures like Regular Linear BK CSA, Modified Linear BK CSA, Regular SQRT BK CSA and Modified SQRT BK CSA are designed for 16-Bit wordsize only. , the timing delay greatly reduces for proposed Vedic multiplier as compared to Vedic multiplier using Mux Based multiplier. The results demonstrate that BKA based Vedic multiplier has delay of 6.13 ns and Vedic multiplier using MUX based full adder has delay of 8.89 ns.

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